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FPGA BASED IMPLEMENTATION OF 32 BIT RISC PROCESSOR

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Abstract

In this paper, a design of general purpose processor with a 5 stage pipeline, to incorporate programmable resources in to a processor. RISC processors have a CPI (clock per instruction) of one cycle. This is due to the optimization of each instruction on the CPU and a technique called pipelining. This technique allows each instruction to be processed in a set number of stages. This in turn allows for the simultaneous execution of a number of different instructions, each instruction being at a different stage in pipeline. The development approach of the overall system design depends on the design specification, analysis and simulation. The RISC Processor core is high performance 32-bit microprocessor. This processor make it especially suited to embedded control applications.

Keywords: Pipeline, clock per instruction, control applications

1. INTRODUCTION

As the high capacity ,low –cost FPGA devices train continues its revolutionary journey through the electronics design Landscape, an ever-increasing number of design landscape, an ever-increasing number of designers are jumping on board trading their traditional hardware-based systems for the attractive ness of the FPGA's 'soft' programmability.

Creation of soft processor based systems, destined to run within a chosen
Target FPGA device, becomes second nature – utilizing one of the many supported flavors of 32 –bit RISC processor, wired up to access peripheral I/O and memory over a standard bus interface.' Soft processors are processors that are defined as part of the FPGA design that is programmed into the physical FPGA device, rather than physical, discrete devices connected to the FPGA, or processors that are immersed as part of the physical FPGA's makeup. Such processors are typically 32-bit and have simple, RISC architectures.

Embedded software refers to the code- the software 'smarts' – that gets downloaded to the physical FPGA device and which will run on a soft processor defined within the FPGA design. The beauty of using 'soft' processors in FPGA designs is that you are not locked to a physical device. We can change processor or modify the code running on it simply by reprogramming the physical FPGA device with a modified hardware design or updated embedded code – leading to true ' field upgradeable hard ware and software'.

2. MICRO ARCHITECTURE

It includes the CPU core, an instruction cache and data cache. You can select an optimum data and instruction cache configuration among a variety of possible configurations.

Micro architectures can be pipelined to different categories. Thus the degree of pipelining is a micro architectural decision.

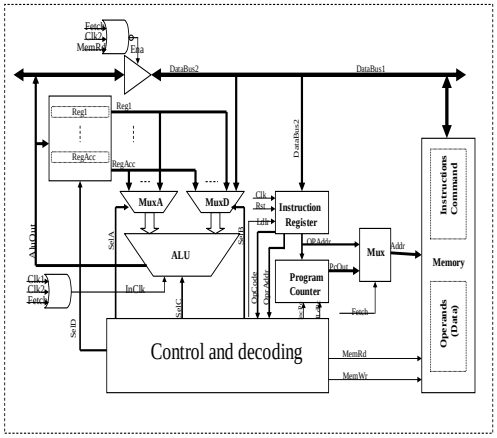


Figure 1: Block diagram of the RISC Processor Core.

Final clock frequency of a specific processor pipeline on a given silicon process technology depends heavily on how deeply the processor is pipelined. When designing a new processor, a key design decision is the target design frequency of operation. The frequency target determines how many gates of logic can be included per pipeline stage in the design. This helps to determine how many pipeline stages there are in the machine.

There are trade offs when the designing for higher clock rates. High clock rates need deeper pipelines so the efficiency at the same clock rate goes down. Deeper pipelines make many things take more clock cycles, such as mispredicted branches and cache misses, but usually more than make up for the lower per-clock efficiency by allowing the design to run at a much higher clock rate. 50%
Increase in frequency might buy only a 30% increase in net performance, nut this frequency increase still provides a significant overall performance increase.

High-frequency design also depends heavily on circuit design techniques, design methodology, design tools, Silicon process technology, power and thermal constrains, etc. At higher frequencies, clock skews and jitter and latch Delay becomes a much bigger percentage of the clock cycles, reducing the percentage of the clock cycle usable by actual logic. The deeper pipelines make the machine more complicated and require it to have deeper buffering to cover the longer pipelines.

The CPU core comprises the following blocks:

CPU register: General purpose register, program counter

CP0 register: Registers for system control coprocessor (cp0) functions

ALU/Shifter: Computational unit

MAC: Computational unit for multiply/add

Bus interface unit: Control bus interface between CPU core and external circuit.

Memory management unit: Direct segment mapping memory management unit.

3. INSTRUCTIONSET OVERVIEW

All Processor Core instructions are 32 bits in length. These are three instruction formats: Immediate (I-type), Jump (j-type) and register (R-type). Having just three instruction formats simplifies instruction decoding.

I-type (Immediate)

31 26	25 21	20 16	15
OP	rs	rt	Immediate

J-type (Jump)

31 26	25
OP	Target

R-type (Register)

31 26	25 21	20 16	15 11	10 6	5
OP	rs	rt	rd	sa	funct

3.1. Load/Store machine with a large number of internal registers:

RISC design philosophy typically uses a large number (commonly 32) of registers. Most instructions operate on these registers, with access to memory made using a very limited set of Load and Store instructions. This limits the need for continuous access to slow memory for loading and stroring data.

3.2 Separate Data Memory and Instruction Memory access paths:

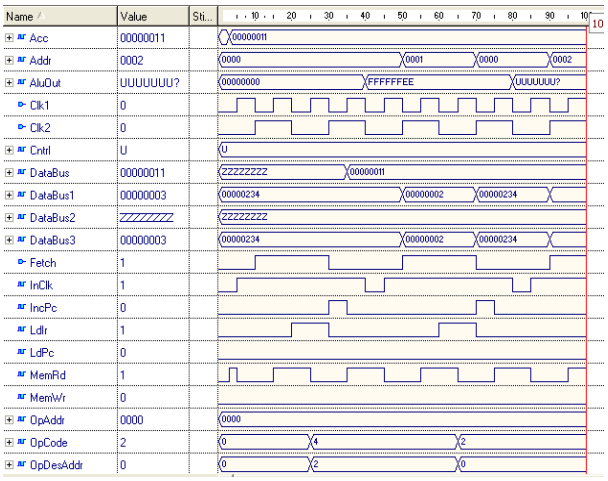
Different stages of the pipeline perform simultaneous accesses to memory. This Harvard style of architecture can either be used with two completely different memory spaces, a single dual-port memory space with separate data and instruction caches for the two pipeline stages.

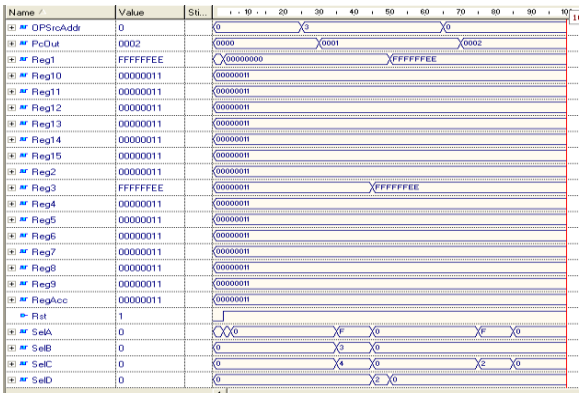
This high-speed ALU core is kept as small as possible to minimize the metal length and loading. Only the essential hardware necessary to perform the frequent ALU operations is included in this high-speed ALU execution loop. Functions that are not used very frequently, for most integer programs, are not put in this key low-latency ALU loop but are put elsewhere. Some examples of integer execution hardware put elsewhere are the multiplier, shifts, flag logic, and branch processing.

The processor does ALU operations with an effective latency of one-half of a clock cycle. It does this operation in a sequence of three fast clock cycles (the fast clock runs at 2x the main clock rate) as shown in Figure 7. In the first fast clock cycle, the low order 16-bits are computed and are immediately available to feed the low 16-bits of a dependent operation the very next fast clock cycle. The high-order 16 bits are processed in the next fast cycle, using the carry out just generated by the low 16-bit operation. This upper 16-bit result will be available to the next dependent operation exactly when needed. This is called a staggered add.

4 SYNTHESIZED RESULTS

The ISA of the 32 bit RISC processor was described using the VHDL .The tool chain including the Active HDL simulator; it was synthesized using Xilinx 9.2i. The total memory usage is 81408 kB. Maximum combinational path delay is 2.677ns. Operating clock frequency about 300 MHZ.





Simulation Results of RISC Processor

5 CONCLUSION

32-bit RISC Processor core has been design and implemented in hardware on Xilinx Spartan 3E FPGA. The design has been achieved using VHDL and simulated with Xilinx 9.2i. Spartan 2E development board has been used for the hardware part. Most of the goals were achieved and simulation shows that the processor is working perfectly, Future work will be added by increasing the number of instructions and make a pipelined design with less

clock cycles per instruction and more improvement can be added in the future work.

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